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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,734	07/16/2003	Sameh W. Asaad	728-236	9040
28249	7590	01/13/2006	(YOR9-2003-0149-U)	
DILWORTH & BARRESE, LLP 333 EARLE OVINGTON BLVD. UNIONDALE, NY 11553			EXAMINER IWASHKO, LEV	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/620,734		ASAAD ET AL.	
	Examiner		Art Unit	
	Lev I. Iwashko		2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 20 and 21 is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>03/18/2004</u> . | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because drawings 1 and 7 have hand-written items and references, making them informal. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, and 7 are rejected under U.S.C. 102(b) as being anticipated by Hansen et al. (US Patent 5,742,840).

Claim 1. A system for instruction memory storage (*Column 4, lines 34 – States that the unit stores data*)

- and processing in a computing device having a processor, (*Column 4, lines 25-30 – Denote a computing device with a processor*)
- the system being based on backwards branch control information, the system comprising: (*Column 4, lines 48-55*)
- a dynamic loop buffer (DLB) organized as a direct-mapped structure, said DLB being a tagless array of data; (*Column 20, lines 23-26 –*

Describe the caches (instruction caches which are also known as DLBs which by definition are tagless) as being directly mapped)

- a DLB controller having a primary memory unit partitioned into a plurality of banks, wherein said controller controls the state of the instruction memory storage system, accepts a program counter address (pc address) as an input, and outputs distinct signals; *(Column 4, lines 62-67 and Column 5, lines 1-9 – State that there are memory controllers which are partitioned into a plurality of elements that are coupled in parallel so that stored memory could be controlled. Bits of data are input (as addresses), and signals are outputted)*
- an address register located in the memory of said computing device, *(Column 5, lines 29-30 – Claim a plurality of registers)*
- wherein said address register is a staging register for said program counter address, *(Column 15, lines 35-38 – Claim a privilege level register (a.k.a. staging register) that for the program counter address)*
- and an instruction fetch process takes two cycles of said processor; *(Column 17, lines 39-40 – State that the instructions can take 2 to 5 cycles to execute)*
- and a bank select unit for serving as a pc-address decoder to accept the program counter address and to output a bank enable signal for selecting a bank in a primary memory unit, and a decoded address for access within the selected bank. *(Column 17, lines 35-46 – State that there is a branch prediction mechanism and instructions are encoded for easy future decoding and access)*

Claim 3. The system of claim 1, wherein said primary memory unit is one of a static random access memory (SRAM) or a dynamic random access memory (DRAM). *(Column 3, line 11 – Denotes a DRAM)*

Claim 7. The system of claim 1, wherein said DLB further includes a read or write port *(Column 6, line 7 – States that there is an input and output port)*

- and accepts three input signals (*Column 21, lines 38-43 – State that three input signals can be accepted due o there being 3 I/O channels*)

4. Claims 10-15 are rejected under U.S.C. 102(b) as being anticipated by Yoshida et al. (US Patent 6,205,536).

- Claim 10. An instruction buffer managing system in a computing system (*Column 13, lines 45-48 – Denote an instruction buffer managing system*)
- including a processor, said system comprising: (*Abstract, line 1 – Claims a processor*)
 - an instruction address input for receiving one or more program counter values from said processor; (*Column 10, lines 5-7 – Denote an instruction address input for fetching a program counter value*)
 - a controllable path between the instruction address input and an instruction address output that passes program counter values to an instruction memory, the instruction memory being connected to the instruction address output, wherein said program counter values received at the instruction address input are monitored; (*Column 9, lines 65-67 and Column 10, lines 1-19 – Describe the Instruction Fetch Unit, and how it includes an instruction address output and input that are connected to an instruction queue where counter values are received and monitored from the address input*)
 - a controller for defining a range of instructions, (*Column 1, lines 63-67 – State that there is a controller for instructions*)
 - the range of instructions comprising a loop; (*Column 7, lines 59-61 – Claim that the addressing mode (which is an instruction) is repeated (which is the definition of a loop)*)
 - and a filler for filling a buffer with each instruction of a range in a first pass, except for at least one unfilled instruction, wherein the program counter values on one or more subsequent loop iterations are

continuously monitored until an unfilled instruction is encountered and a buffer manager provides said unfilled instruction. *(Column 12, lines 38-58 – Describe the store buffer (filling buffer) and how it is filled with instructions in a pipeline manner)*

- Claim 11. A system of claim 10, wherein said unfilled instructions are within a sub range defined by a forward non-consecutive control flow instruction. *(Column 12, lines 47-58, Declare instructions that are unfilled, due to the fact that they cannot be processed by one-time pipelineing. The decoding stage separate the instructions into a plurality of step codes)*
- Claim 12. A system of claim 10, wherein said unfilled instructions are within a sub range defined by a backward non-consecutive control flow instruction. *(Column 12, lines 47-58, Declare instructions that are unfilled, due to the fact that they cannot be processed by one-time pipelineing. The decoding stage separate the instructions into a plurality of step codes)*
- Claim 13. A system of claim 10, wherein an instruction address of said unfilled instructions fall outside a sequential address associated with the buffer and are therefore omitted. *(Column 13, lines 12-20 – State that the instructions are omitted EIT is detected in any stage besides the “E” stage)*
- Claim 14. A system of claim 13, wherein the buffer manager takes unfilled instruction from the instruction memory. *(Column 15, lines 11-17 – State that the store buffer takes the operand during a gap of a microstep)*
- Claim 15. A system of claim 10, wherein instructions in the buffer are retained after the processor fetches instructions outside the range. *(Column 12, lines 38-41 – Describe the store buffer (filling buffer) and how it retains instructions)*

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2 and 6 are rejected under 35 U.S.C.103(a) as being unpatentable over Hansen et al. as applied to claims 1 above, further in view of Chung et al. (US PGPub 2002/0178350 A1).

Hansen teaches the limitations of claim 1 for the reasons above.

Hansen's invention differs from the claimed invention in that there is no specific reference to a multiplexors or latches.

Hansen fails to teach claims 2.

The first part of claim 2 states: "The system of claim 1, further comprising: "a first multiplexor for selecting amongst a plurality of banks of said primary memory unit;". Chung declares "The LBF registers are also read through a multiplexer 135 with the same four LSBs of program address 140 used as select signals" (Section 0024, lines 9-11).

The second part of claim 2 states: "a second multiplexor for selecting between the DLB and the primary memory unit output;". Chung declares "the active signal is used to select multiplexer 126, which multiplexes between the instruction read from either loop buffer 122 or main program memory 130" (Section 0024, lines 14-16).

The third part of claim 2 states: "a latch for staging the data; and a data-out register located in the main memory of said computing device, wherein said data-out register receives instruction data for said processor at the decode stage". Chung declares "If the instruction retrieved from loop buffer 122 is a coprocessor type instruction, the output of multiplexer 126 is latched into coprocessor instruction register latch 128, decoded by decoder 125 and executed by operation execution unit 127 of coprocessor 120" (Section 0024, lines 36-40).

Hansen fails to teach claim 6, which states: "The system of claim 2, wherein said distinct signals output from said DLB controller include: signals to enable/disable said processor to access said primary memory unit, to read the DLB and to write the DLB; decoded address signals for said processor to access said DLB; and select signals to select a first multiplexor." Chung declares the following: "Referring again to FIG. 3, the latches of loop buffer 122 are shown to be addressed by the LSBs of program address 140 for writing the instructions of the loop routine fetched from main program memory 130. In the next iteration of the same loop routine, the instructions are read out of loop buffer 122, the reading of the instructions from the latches of loop buffer 122 are through a 'm to 1' multiplexer 133, with the select port addressed by the 4 LSBs of program address 140" (Section 0024, lines 1-9).

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Programmable Media Processor" of Hansen and Chung's "Loop Instruction Processing" before him at the time the invention was made, to combine the two inventions so that the system would include multiplexers for selection and latches for staging the data in order to ensure system efficiency and reduce the time for operations to occur.

7. Claim 4 is rejected under 35 U.S.C.103(a) as being unpatentable over Hansen et al. as applied to claim 1 above, further in view of Gold et al. (US Patent 5,926,840).

Hansen teaches the limitations of claim 1 for the reasons above.

Hansen 's invention differs from the claimed invention in that there is no specific reference to a Growable Register Array.

Hansen fails to teach claim 1, which states: "The system of claim 1, wherein said DLB is made of energy efficient growable register arrays (GRAs)." However, Gold 's invention

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discloses that “In a preferred embodiment, memory fetch list 302 is a 4-port Growable Register Array (GRA) implemented as embedded RAM” (Column 3, lines 56-58). It would have been obvious to one of ordinary skill in the art, having the teachings of the “Programmable Media Processor” of Hansen and Gold 's “Out-of-Order Fetching” before him at the time the invention was made, to include a Growable Register Array in order to preserve space, speed and efficiency in the system.

8. Claim 5 is rejected under 35 U.S.C.103(a) as being unpatentable over Hansen et al. as applied to claim 1 above, further in view of Dean (US Patent 5,544,342).

Hansen teaches the limitations of claim 1 for the reasons above.

Hansen 's invention differs from the claimed invention in that there is no specific reference to register array cells.

Hansen fails to teach claim 1, which states: “The system of claim 1, wherein said DLB is made of energy efficient register array cells.” However, Dean 's invention discloses that “FIG. 28a is a floor plan diagram of STRiP's register file 418. FIG. 28b is a schematic electrical circuit diagram of a memory cell of the register array” (Column 44, lines 36-38). It would have been obvious to one of ordinary skill in the art, having the teachings of the “Programmable Media Processor” of Hansen and Dean 's “System and Method for Prefetching Information in a Processing System” before him at the time the invention was made, to include register array cells in order to preserve space, speed and efficiency in the system.

9. Claims 8 and 9 are rejected under 35 U.S.C.103(a) as being unpatentable over Hansen et al. and Chung et al. (US PGPub 2002/0178350 A1).

Hansen teaches a portion of claim 8: “A method of instruction memory storage”, with the following: “...stored data...” (Column 4, lines 34).

Hansen further teaches a portion of claim 8: “and processing in a computing device having a processor”, with the following: “According to another aspect of the invention, a general purpose programmable media processor is provided having an instruction path and a data path to digitally process a plurality of media data streams. The media processor includes a high bandwidth external interface operable to receive a plurality of data of various sizes from an external source” (Column 4, lines 25-30).

Hansen further teaches a portion of claim 8: “a dynamic loop buffer (DLB)”, with the following: “The preferred embodiment also includes a combined instruction cache and buffer that is dynamically allocated between cache space and buffer space to ensure real-time execution of multiple media instruction streams, and a combined data cache and buffer that is dynamically allocated between cache space and buffer space to ensure real-time response for multiple media data streams” (Column 4, lines 55-61).

Hansen further teaches a portion of claim 8: “and a DLB controller, the method being based on backwards branch control information, the method comprising the steps of:”, with the following: “Means are also provided for securely controlling the sequence of execution by performing branch and gateway operations based upon instructions and data received by the execution unit. A memory management unit operable to retrieve data and instructions for timely and secure communication over the data path and instruction path respectively is also preferably included in the media processor” (Column 4, lines 48-55).

Hansen further teaches a portion of claim 8: “and completing and output data in a data register in one clock cycle”, with the following: “...releasing the serial data in the next cycle...” (Column 25, lines 21-22).

Chung teaches a portion of claim 8: “measuring cycles from a valid program counter address latched from an address register to valid data; latching said program counter address said DLB controller and a bank select unit from said address register at a rising edge of every clock cycle; said DLB controller and said bank select unit processing signals for data access during a first half of the clock cycle;” latching signals at the DLB and at a primary memory unit on the falling edge of the clock cycle;” with the following: “A first latch responds to phase 1 and a second latch responds to phase 2 of the system clock” (Section 0019, lines 7-10).

Hansen fails to teach claim 9, which states: “A method of claim 8, further comprising a step of latching data from a data register to a data-out and to the DLB for storing at the falling edge of the clock, when said controller is in a FILL state.” Chung declares the following: “Referring again to FIG. 3, the latches of loop buffer 122 are shown to be addressed by the LSBs of program address 140 for writing the instructions of the loop routine fetched from main program memory 130. In the next iteration of the same loop routine, the instructions are read out of loop buffer 122, the reading of the instructions from the latches of loop buffer 122 are through a ‘m to 1’ multiplexer 133, with the select port addressed by the 4 LSBs of program address 140” (Section 0024, lines 1-9). Chung also declares the following: “A first latch responds to phase 1 and a second latch responds to phase 2 of the system clock” (Section 0019, lines 7-10).

It would have been obvious to one of ordinary skill in the art, having the teachings of the “Programmable Media Processor” of Hansen and Chung's “Loop Instruction Processing” before

him at the time the invention was made, to combine the two inventions so that the system would include latches for staging the data in order to ensure system efficiency and reduce the time for operations to occur.

10. Claim 16 is rejected under 35 U.S.C.103(a) as being unpatentable over Yoshida et al., further in view of Lee et al. (US Patent 6,401,196) and Dayan (US PGPub 2004/0268047).

Yoshida teaches a portion of Claim 16, “A method of changing states of a dynamic loop buffer (DLB) controller having four states, to enable limiting a use of energy in a computing device”, with the following: “...waiting state (input waiting)...” (Column 15, line 42). “...waiting state (output waiting)...” (Column 15, lines 45-46). “an instruction read cycle with one wait state (C4)...” (Column 16, lines 65-66). “...a data read cycle with one state (C6)...” (Column 16, lines 66-67).

Yoshida teaches a portion of Claim 16, “having a processor, a DLB, and the DLB controller, while said computing device is performing instruction memory storage and processing”, with the following: “CPU 71 accesses instruction cache 72 by sending/receiving control signals through an instruction control bus 83” (Column 1, lines 63-65).

Lee teaches a portion of Claim 16, “using backwards branch control information, the method comprising the steps of:”, with the following: “The first state, IDLE state 40, indicates that a short backward branch (SBB) has not been detected” (Column 5, lines 45-46).

Lee further teaches a portion of Claim 16, “in an initial IDLE state, determining if a back branch was taken;”, with the following: “The first state, IDLE state 40, indicates that a short backward branch (SBB) has not been detected” (Column 5, lines 45-46).

Lee further teaches a portion of Claim 16, “and entering an ACTIVE state if the

determination is positive”, with the following: “Upon detection of an SBB, and if the SBB is taken, the state machine will of branch control 34 exits IDLE state and enters ACTIVE state” (Column 5, lines 46-48).

Lee further teaches a portion of Claim 16, “and if the determination is negative, returning to the IDLE state.”, with the following: “The state machine will return to the IDLE state when one of the following two conditions is met: (1) the detected SBB instruction that triggered the transition from an IDLE state to an ACTIVE state is not taken” (Column 5, lines 55-59).

Dayan teaches a portion of Claim 16, “entering a FILL state if the determination is positive, and if the determination is negative, determining if an unfilled entry was hit;”, with the following: “The present invention proposes a flexible data, cache line fill policy that takes into account repeated memory string operations including the current state of the DF” (Section 0024, lines 1-4). “The read miss operation 30 is initiated when an addressed doubleword is not present in the cache” (Section 0026, lines 4-6).

Dayan teaches a portion of Claim 16, “entering the FILL state if the determination is positive, and if the determination is negative, determining if a filled entry was hit;”, with the following: “The present invention proposes a flexible data, cache line fill policy that takes into account repeated memory string operations including the current state of the DF” (Section 0024, lines 1-4). “The read miss operation 30 is initiated when an addressed doubleword is not present in the cache” (Section 0026, lines 4-6).

It would have been obvious to one of ordinary skill in the art, to combine the “Caching System” of Yoshida, Lee’s “Data Processing System” and Dayan’s “Method and System for

Cache Data Fetch Operations” so that a more efficient and inclusive method would be created for limiting the energy use in a DLB.

11. Claims 17-19 are rejected under 35 U.S.C.103(a) as being unpatentable over Yoshida et al., Lee et al. and Dayan.

Yoshida, Lee and Dayan teach the limitations of claim 16 for the reasons above.

Yoshida's and Lee's inventions differ from the claimed invention in that there is no specific reference to a FILL state.

Lee's and Dayan's inventions differ from the claimed invention in that there is no specific reference to an OVERFLOW state.

Yoshida, Dayan and Lee fail to teach portions of claims 17-19, which respectively state “The method of claim 16, further comprising the steps of: in the FILL state, determining if an address is out of range; entering the IDLE state if the determination is positive, and if the determination is negative, determining if a filled entry was hit, entering the ACTIVE state if the determination is positive, if the determination is negative, determining if an offset is greater than a physical address; and entering an OVERFLOW state if the determination is positive, if the determination is negative returning to the FILL state”, “The method of claim 17, further comprising the steps of: in the ACTIVE state determining if the address is out of range; entering the IDLE state if the determination is positive, and if the determination is negative, determining if an unfilled entry was hit; and entering the FILL state if the determination is positive, and if the determination is negative, determining if an offset is greater than a physical address; and entering the OVERFLOW state if the determination is positive, and if the determination is negative returning to the ACTIVE state”, and “The method of claim 17, further comprising the

steps of: in the OVERFLOW state, determining if an unfilled entry was hit; entering an FILL state if the determination is positive, and if the determination is negative, determining if a filled entry was hit; and entering the ACTIVE state if the determination is positive, and if the determination is negative, returning to the OVERFLOW state.”

Dayan states the following: “If the DF indicates an incrementing address operation and the targeted memory's address is the highest address in the current cache line in memory, then the data is written directly to memory, and there is no cache fill for the current targeted memory address cache line, and instead the next (or higher) cache line is filled into the cache. Similarly, if the DF indicates a decrementing address operation and the targeted memory's address is the lowest address in the current cache line in memory, then the data is written directly to memory and there is no cache fill for the current targeted memory address cache line, and instead the previous (or lower) cache line is filled into the cache” (Section 0029, lines 14-25).

Yoshida states the following: “The size of a source operand in a register is fixed at 32 bits. Where the size of the register operand differs from the memory operand and the source operand side is larger, the operand is shortened by the overflow portion and an overflow check is done” (Column 6, lines 15-19).

It would have been obvious to one of ordinary skill in the art, to combine the “Caching System” of Yoshida, Lee’s “Data Processing System” and Dayan’s “Method and System for Cache Data Fetch Operations” so that a more efficient and inclusive method would be created for limiting the energy use in a DLB.

Allowable Subject Matter

12. Claims 20 and 21 are allowed.

The following is an examiner's statement of reasons for allowance:

Claim 20 and 21 are respectively "A method of changing states of a dynamic loop buffer (DLB) controller having four states" and "A computer program device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for a method of changing states of a dynamic loop buffer (DLB) controller having four states". The rest of claims 20 and 21 are identical, so it is acceptable to only reference the items in the claims once for the duration of this explanation.

The rest of the claims reads as follows: "to enable limiting a use of energy in a computing device having a processor, a DLB, and the DLB controller, while said computing device is performing instruction memory storage and processing using backwards branch control information, the method comprising the steps of: in a FILL state fetching instruction packets from a primary memory unit, writing a copy of said instruction packets into a DLB, setting a valid bit to assert validity of said DLB, entering an ACTIVE state when a backward branch is taken within a range of a loop, entering an IDLE state when said backward branch completes a loop and a change of flow branch is taken out of range of said loop, and entering an OVERFLOW state if the DLB fills up and said change of flow branch is not taken; in the ACTIVE state presenting instruction fetches to the DLB, entering the IDLE state if said backward branch is not taken and a change of flow branch is taken out of range, entering the FILL state if the buffer is not full, if said backward branch is within the loop, entering an OVERFLOW state if the buffer is full, entering the FILL state if the buffer is full, and entering the OVERFLOW state if the end of the buffer is reached said and change of flow branch is not taken; in the OVERFLOW state reading instruction data packets from a primary memory unit of

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said computing device, entering the IDLE state after performing a jump or a branch instruction out of range of said loop; entering the ACTIVE state if said backward branch is taken, entering the ACTIVE state if a backward branch within the range of said loop is taken and data is valid, and entering the FILL state if a backward branch within the range of said loop is taken and data is invalid; and in the IDLE state accessing instruction data packets from the primary memory unit, entering the FILL state if a new backward branch is detected, and entering the ACTIVE state if a last loop captured in the dynamic loop buffer is repeated.”

Since every state (FILL, IDLE, OVERFLOW and ACTIVE) is so well-defined in a step-by-step fashion, there is great difficulty in finding prior art that will object to the entirety of the claim. Even by combining the prior art of Hansen et al. (US Patent 5,742,840), Yoshida et al. (US Patent 6,205,536), Lee et al. (US Patent 6,401,196) and Dayan (US PGPub 2004/0268047), it is not possible to overcome every aspect of claims 20 and 21. For instance, none of the prior art mentions “change of flow” or “entering the ACTIVE state if a last loop captured in the dynamic loop buffer is repeated”.

Therefore, claims 20 and 21 are allowed due to their specific nature and because they both overcome obviousness.

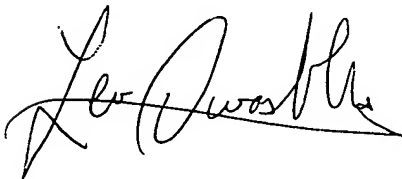
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lev Iwashko



MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100